IN THE CLAIMS

A listing of the pending claims is shown below. Claims 15, 16, and 18 are currently amended and new claims 30-40 are added.

1-12. (Cancelled)

13. (Original) A system comprising:

a die including an electronic system;

a capacitor located less than about .1 millimeter from the die and coupled to the die, the capacitor is capable of decoupling a power supply connection at the die without additional capacitors located external to the die; and

a dielectric layer located between the capacitor and the die.

14. (Original) The system of claim 13, wherein the dielectric layer has a thickness of between about .05 millimeters and about .1 millimeters.

15. (Currently Amended) A system comprising:

a first die;

a second die; and

a capacitor <u>including a plurality of plated through holes coupling at least four conductive layers embedded in a dielectric to a plurality of connection cites</u> and having a first surface having a controlled collapse chip connection coupled to the first die and a second surface having a controlled collapse chip connection coupled to the second die.

16. (Currently Amended) A system comprising:

a first die;

a second die; and

a capacitor having a first surface having a controlled collapse chip connection coupled to the first die and a second surface having a controlled collapse chip connection coupled to the second die, ~~The system of claim 15,~~ wherein the first die includes a processor and the second die includes a communication system.

17. (Canceled)

18. (Currently Amended) A system comprising:

a substrate having a first surface and a second surface;

a die coupled to the first surface; and

a capacitor having a plurality of ~~vias~~ plated through holes coupled to a plurality of conductive layers in the capacitor, the capacitor is coupled to the second surface by a controlled collapse chip connection and the capacitor is electrically coupled to the die through the substrate.

19. (Original) The system of claim 18, wherein the die includes a processor.

20. (Original) The system of claim 19, wherein the die has a die surface and the capacitor has a capacitor surface and the capacitor surface is located less than about .1 millimeter from the die surface.

21. (Original) A system comprising:

a processor requiring at least 5 watts of power to be operable; and

a single multilayered single package capacitor coupled to the processor and capable of decoupling a power supply from the processor.

22. (Original) The system of claim 21, wherein the single multilayered single package capacitor is capable of being mounted on a substrate by a plurality of solder bumps.

23. (Original) The system of claim 22, wherein the single multilayered capacitor is capable of being mounted on a substrate using a controlled collapse chip connection.

24-29. (Cancelled)

30. (New) The system of claim 13, wherein the capacitor comprises palladium.

31. (New) The system of claim 30, wherein the capacitor comprises barium titanate.

32. (New) The system of claim 31, wherein the barium titanate is formed from sheets having a thickness of between about five and about seven microns.

33. (New) The system of claim 15, wherein the at least four conductive layers comprise platinum.

34. (New) The system of claim 33, wherein the first die comprises silicon.

35. (New) The system of claim 16, wherein the capacitor comprises a plurality of dielectric sheets having at least two different thicknesses.

36. (New) The system of claim 35, wherein the first die and the second die comprise silicon.

37. (New) The system of claim 18, wherein the capacitor includes a high voltage site surrounded by four low voltage sites.

38. (New) The system of claim 37, wherein each of the plurality of conductive layers comprises palladium.

39. (New) The system of claim 21, wherein the single multilayered single package capacitor comprises barium titanate.

40. (New) The system of claim 39, wherein the single multilayered single package capacitor comprises platinum.